IN THE CLAIMS

1. (Previously presented) A method comprising:

forming a process layer above a semiconducting substrate;

etching at least a portion of said process layer;

measuring a first depth of the etch at a first location in a first preselected region of a plurality of preselected regions of the semiconducting substrate, wherein each of the plurality of preselected regions of the semiconducting substrate has an associated temperature adjusting element;

comparing the first depth to a desired depth;

providing an indication to the temperature adjusting element associated with the first preselected region to adjust the temperature in response to the first depth being different from the desired depth; and

adjusting the temperature of at least a portion of the first preselected region in response to receiving the indication.

2. (Previously presented) A method, as set forth in claim 1, further comprises:

measuring the depth of the etch at a second location in a second preselected region of the semiconducting substrate;

comparing the second depth to a second desired depth; and

providing a second indication to a second temperature adjusting element associated with the second preselected region to adjust the temperature in response to the second depth being different from the second desired depth; and

adjusting the temperature of at least a portion of the second preselected region in response to receiving the second indication.

3. (Original) A method, as set forth in claim 1, wherein comparing the first depth to a desired depth further comprises:

measuring a second depth of the etch at a second location in a second preselected region of the semiconducting substrate; and

setting the desired depth to the second depth.

4. (Previously presented) A method, as set forth in claim 2, wherein varying the temperature comprises raising the temperature of the subsequently processed semiconducting substrate in the region corresponding to the second preselected region in response to the second depth being less than the desired depth.

5. (Previously presented) A method, as set forth in claim 1, wherein the temperature adjusting element is a cooling element, wherein adjusting the temperature comprises lowering the temperature of at least the portion of the first preselected region.

6. (Original) A method, as set forth in claim 1, wherein forming a process layer above a semiconducting substrate comprises forming a process layer comprised of at least one of an oxide, an oxynitride, polysilicon, and a metal above a semiconducting substrate.

7. (Original) A method, as set forth in claim 1, wherein etching at least a portion of said process layer further comprises performing a plasma etching process on at least a portion of the process layer.

8. (Previously presented) A method, as set forth in claim 1, wherein the temperature adjusting element is a heating element, wherein adjusting the temperature comprises raising the temperature of at least the portion of the first preselected region.

9. (Original) A method, as set forth in claim 1, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

averaging the plurality of measured depths to determine the first depth.

10. (Original) A method, as set forth in claim 1, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the smallest measured depth to be the first depth.

11. (Original) A method, as set forth in claim 1, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the greatest measured depth to be the first depth.

12. (Original) A method, as set forth in claim 1, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the median measured depth to be the first depth.

13. (Previously presented) A method comprising:

forming a process layer above a semiconducting substrate;

etching at least a portion of said process layer;

measuring a depth of the etch at a plurality of locations in a first preselected region of the semiconducting substrate;

measuring a depth of the etch at a plurality of locations in a second preselected region of the semiconducting substrate;

determining if at least a portion of the first preselected region is etched to a first desired depth based on the measured depth of the plurality of locations in the first preselected region;

varying the temperature of a subsequently processed semiconducting substrate in a region corresponding to the first preselected region in response to determining the at least the portion of the first preselected region is not etched to the first desired depth;

determining if at least a portion of the second preselected region is etched to a second desired depth based on the measured depth of the plurality of locations in the second preselected region; and

varying the temperature of a subsequently processed semiconducting substrate in a region corresponding to the second preselected region in response determining the at

least the portion of the second preselected region is not etched to the second desired depth.

14. (Previously presented) A method, as set forth in claim 13, wherein varying the temperature further comprises raising the temperature of the subsequently processed semiconducting substrate in the region corresponding to the second preselected region in response to determining the at least the portion of the second preselected region is etched less than the second desired depth.

15. (Previously presented) A method, as set forth in claim 13, wherein varying the temperature further comprises raising the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region in response determining the at least the portion of the first preselected region is etched less than the first desired depth.

16. (Original) A method, as set forth in claim 13, wherein forming a process layer above a semiconducting substrate comprises forming a process layer comprised of at least one of an oxide, an oxynitride, polysilicon, and a metal above a semiconducting substrate.

17. (Original) A method, as set forth in claim 13, wherein etching at least a portion of said process layer further comprises performing a plasma etching process on at least a portion of the process layer.

18. (Previously presented) A method, as set forth in claim 13, wherein varying the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region comprises varying the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region as a function of the difference.

19. (Previously presented) A method, as set forth in claim 13, wherein measuring the depth at the plurality of locations in the first preselected region comprises averaging the plurality of measured depths, and wherein determining if at least the portion of the first preselected region is etched to the first desired depth comprises comparing the average of the plurality of the measured depths to the first desired depth.

20. (Previously presented) A method, as set forth in claim 13, wherein measuring the depth at the plurality of locations in the first preselected region comprises determining the smallest measured depth of the plurality of measured depths, and wherein determining if at least the portion of the first preselected region is etched to the first desired depth comprises comparing the smallest measured depth of the plurality of the measured depths to the first desired depth.

21. (Previously presented) A method, as set forth in claim 13, wherein measuring the depth at the plurality of locations in the first preselected region comprises determining the greatest measured depth of the plurality of measured depths, and wherein determining if at least the portion of the first preselected region is etched to the first desired depth comprises comparing the greatest measured depth of the plurality of the measured depths to the first desired depth.

22. (Previously presented) A method, as set forth in claim 13, wherein measuring the depth at the plurality of locations in the first preselected region comprises determining a median of the plurality of measured depths, and wherein determining if at least the portion of the first preselected region is etched to the first desired depth comprises comparing the median of the plurality of the measured depths to the first desired depth.

23. (Original) A method comprising:

forming a process layer above a semiconducting substrate;

etching at least a portion of said process layer;

measuring a first depth of the etch at a first location in a first preselected region of the semiconducting substrate;

measuring a second depth of the etch at a second location in a second preselected region of the semiconducting substrate;

comparing the first depth to the second depth;

varying the temperature of a subsequently processed semiconducting substrate in a region corresponding to the first preselected region in response to the first depth being different from the second depth.

24. (Original) A method, as set forth in claim 23, wherein varying the temperature further comprises raising the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region in response to the first depth being less than the second depth.

25. (Original) A method, as set forth in claim 23, wherein varying the temperature further comprises lowering the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region in response to the first depth being greater than the second depth.

26. (Original) A method, as set forth in claim 23, wherein forming a process layer above a semiconducting substrate comprises forming a process layer comprised of at least one of an oxide, an oxynitride, polysilicon, and a metal above a semiconducting substrate.

27. (Original) A method, as set forth in claim 23, wherein etching at least a portion of said process layer further comprises performing a plasma etching process on at least a portion of the process layer.

28. (Original) A method, as set forth in claim 23, wherein varying the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region further comprises varying the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region as a function of the difference.

29. (Original) A method, as set forth in claim 23, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

averaging the plurality of measured depths to determine the first depth.

30. (Original) A method, as set forth in claim 23, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the smallest measured depth to be the first depth.

31. (Original) A method, as set forth in claim 23, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the greatest measured depth to be the first depth.

32. (Original) A method, as set forth in claim 23, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the median measured depth to be the first depth.

Claims 33-40 have been previously withdrawn.

41. (New) A method, as set forth in claim 13, further comprising a second semiconductor substrate be processed, and wherein varying the temperature of the subsequently processed semiconductor substrate comprises varying the temperature of the second semiconductor substrate.

42. (New) A method, as set forth in claim 23, further comprising a second semiconductor substrate be processed, and wherein varying the temperature of the subsequently processed semiconductor substrate comprises varying the temperature of the second semiconductor substrate.